Code.No: 43216 | R07 | SET-3

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
II.B.TECH - I SEMESTER REGULAR EXAMINATIONS NOVEMBER, 2009
DIGITAL LOGIC DESIGN
(Common to CSE, IT, CSS)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1. a) Construct a table for 4-3-2-1 weighted code and translate it to 9154 code.
   b) What is the dual of the given Boolean function.
   i) $f = AC + B(\overline{\overline{D} + A})$ $F_2 = (\overline{A} + \overline{B}).C + D.\overline{C}$ [8+8]

2. a) Simplify the following function
   $(x+y)\overline{\left[\overline{x(\overline{y}+\overline{z})}\right]} + \overline{x}\,\overline{y} + \overline{x}\,\overline{z}$
   b) Prove that $wx + \overline{y}(\overline{w} + \overline{z}) = wx + xz + \overline{x}\,\overline{z} + \overline{w}\,\overline{y}z$ if $\overline{w}x + y\overline{z} = 0$. [8+8]

3. If $f = \sum(5,6,13)$ and $f_1 = \sum(0,1,2,3,5,6,8,9,10,11,13)$
   a) Find f_2 such that $f = f_1.f_2$
   b) Realize EX-OR and EX-NOR gates of two input using minimum number of NAND and NOR gates respectively. [16]

4. a) Design a 4 bit BCD adder using Full adder circuits
   b) Write HDL program to model a 3 to 8 decodes using 2 to 4 and 1 to 2 decodes. [8+8]

5 a) Convert a T flip flop to D type flip flop
   b) Show that the characteristic equation for the compliment output of JK flip flop is
   $\overline{Q}(T+1) = \overline{J}.\overline{Q}(t) + K.Q(t)$. [8+8]

6. a) Design an asynchronous up/down counter of 4 bit.
   b) Write HDL code to model the above design. [8+8]

7. Tabulate the truth table for 8*4 ROM to input the following functions:
   $A = \sum(1,2,4,6)$; $B = \sum(0,1,6,7)$
   $C = \sum(2,6)$; $D = \sum(1,2,3,5,7)$ [16]

8. Write a brief note on
   a) Hazards and races
   b) Asynchronies Vs Synchronous sequential circuit. [8+8]

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